IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735.
PP 158-161
www.iosrjournals.org

Hardware Reduction in Data Path Circuits Using Carry Save Arithmetic With Fused Add Multiply Add Architecture

S.Sowndhariya[1], N.Porutselvam [2]
[1](Student,Gnanamani College Of Technology,Namakkal)
[2](Ap/Ece, Gnanamani College Of Technology, Namakkal)

Abstract *:* A high-performance data-path to implement DSP kernels is introduced in this paper. The proposed architecture of data-path is realized by FAMA (Fused Add-Multiply-Add (FAMA) unit). We differentiate from previous works on flexible computational unit using addition and subtraction process it takes that extra hardware. A mapping methodology, for datapath composed with the proposed flexible unit.it exploits the features of proposed units and enables fast computations. Comparing them with the datapath which use existing schemes, the proposed technique yields considerable reductions in terms of area and power consumption in datapath.

Keywords*: Arithmetic optimizations, carry-save (CS) form, datapath synthesis, flexible accelerator, operation chaining, FAMA unit.*

I. INTRODUCTION

Digital Signal Processing (DSP) and multimedia applications, usually spend most of their time executing a small number of code segments with well-defined characteristics are called kernel. To accelerate the execution of such kernels, various high-performance data-paths have been proposed. The incorporation of heterogeneity through specialized hardware accelerators improves performance and reduces energy consumption. Although the specific application integrated circuit (ASICs) form the ideal acceleration solution in terms of performance, area and power, their inflexibility to increased silicon complicity ,as multiple instantiated ASICs are needed to accelerate various kernels..

In timing-driven optimizations based on carry-save (CS) arithmetic were performed at the post- register Transfer Level (RTL) design stage CS optimization is bounded to merging only additions/subtractions. In common sub expression elimination in CS computations is used to optimize linear DSP circuits. The proposed architecture comprises Fused Add- Multiply-Add (FAMA) units which enable the execution of a large set of operation templates found in DSP kernels.

In this brief, we propose a high-performance architectural scheme for the synthesis of flexible hardware DSP accelerators by combining optimization techniques from both the architecture and arithmetic levels of abstraction. We introduce a flexible datapath architecture that exploits CS optimized templates of chained operations. The proposed architecture comprises Fused Add-Multiply-Add (FAMA) unit, which enable the execution of a large set of operation templates found in DSP kernels. The proposed accelerator architecture delivers 1.10% in area-delay and 1% in energy consumption compared to datapath.

II. EXISTING FCU SYSTEM

The existing flexible accelerator architecture is shown in Fig.1. Each FCU operates directly on CS operands and produces data in the same form for direct reuse of intermediate results. Each FCU operates on 16-bit operands. Such a bit-length is adequate for the most DSP data-paths, but the architectural concept of the FCU can be straightforwardly adapted for smaller or larger bit-lengths. The number of FCUs is determined at design time based on the ILP and area constraints imposed by the designer. Which enable the execution of a large set of operation templates found in DSP kernels.

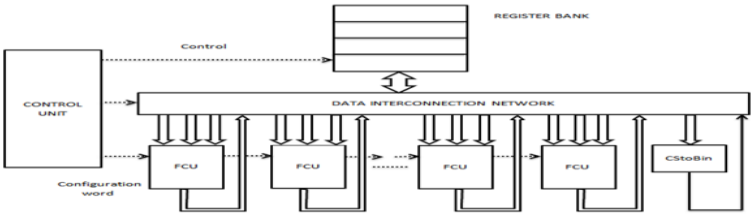

Fig 1: Existing Abstract form of Flexible datapath

The structure of the FCU has been designed to enable high-performance flexible operation chaining based on a library of operation templates.

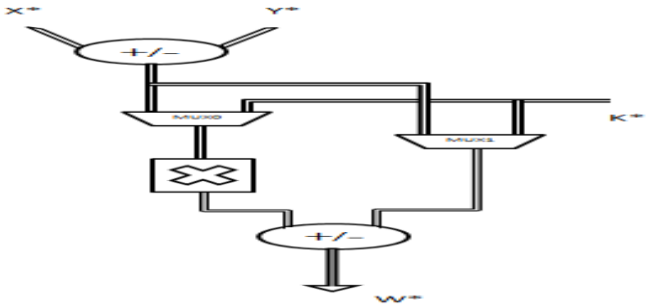

Fig 2 Abstract view of FCU

Each FCU can be configured to operation templates shown in Fig. 2. The proposed FCU enables intra template operation chaining by fusing the additions. The FCU is able to operate on either CS or two's complement formatted operands, since a CS operand comprises two 2's complement binary numbers. FCU template library performed before/after the multiplication and performs partial operation template of the following complex operations.

$W^* = A \times (X^* + Y^*) + K^*$ (1)

$W^* = A \times K^* + (X^* + Y^*)$ (2)

The following relation holds for all CS data: $X^* = \{XC, XS\} = XC + XS$. The operand A is a two's complement number.

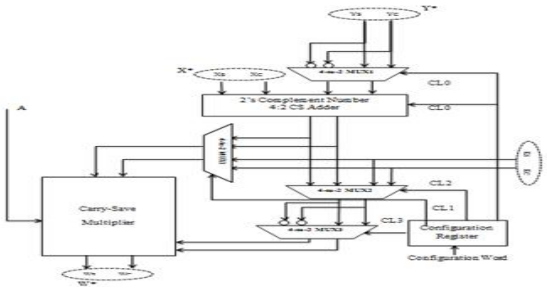

Fig 3. FCU

The alternative execution paths in each FCU are specified after properly setting the control signals of the multiplexers MUX1 and MUX2 (Fig. 3). The multiplexer MUX0 outputs Y * when CL0 = 0 (i.e., X* + Y * is carried out) or Y * when X* − Y* is required and CL0 = 1. The two's complement 4:2 CS adder produces the N* = X* +Y * when the input carry equals 0 or the N* = X* −Y * when the input carry equals 1. The MUX1 determines if N* (1) or K* (2) is multiplied with A. The MUX2 specifies if K* (1) or N* (2) is added with the multiplication product. The multiplexer MUX3 accepts the output of MUX2 and its 1's complement and outputs the former one when an addition with the multiplication product is required (i.e., CL3 = 0) or the later one when a subtraction is carried out (i.e., CL3 = 1). The 1-bit ace for the subtraction is added in the CS adder tree. The multiplier comprises a CS-to-MB module, which adopts a recently proposed technique to recode the 17-bit P* in its respective MB digits with minimal carry propagation. The multiplier's product consists of 17 bits. The multiplier includes a compensation method for reducing the error imposed at the product's accuracy by the truncation technique.

III. PROPOSED FAMA UNIT

The FAMA architecture are shown in Fig 4. The FAMA consist of two mux, two 4:2 CS adder, Carry Save Multiplier, one configuration word. FAMA operates can directly on Carry save operands and produces data in the same form 1 for direct reuse of intermediate results. Each FAMA operates on 16-bit operands. Such a bit-length is adequate for the most DSP datapath, but the architectural concept of the FAMA can be straightforwardly adapted for smaller or larger bit-lengths.

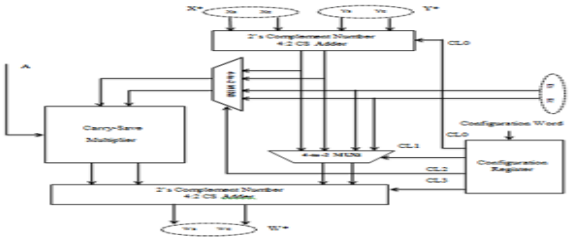

Fig 4 Detailed view of FAMA

The structure of the FAMA has been designed to enable high-performance flexible operation changing based on a library of the operation templates. In each FAMA can be configured to any of the operation templates T1-T5. The proposed FAMA enables intra template operation chaining by fusing the additions and subtraction performed before /after the multiplication.

$Z^* = N^* \times A + K^*$

$N^* = X^* + Y^*$

$X^* = \{X^c, X^s\} = X^c + X^s$

$Y^* = \{Y^c, Y^s\} = Y^c + Y^s$

IV. EXPERIMENTAL RESULT

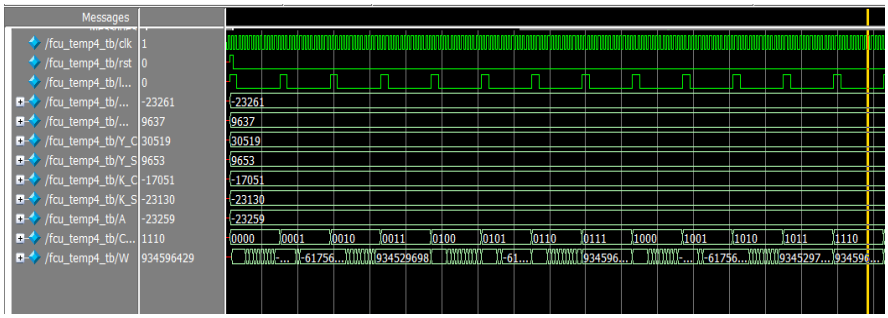

Fig 5: Simulation Result of Proposed FCU

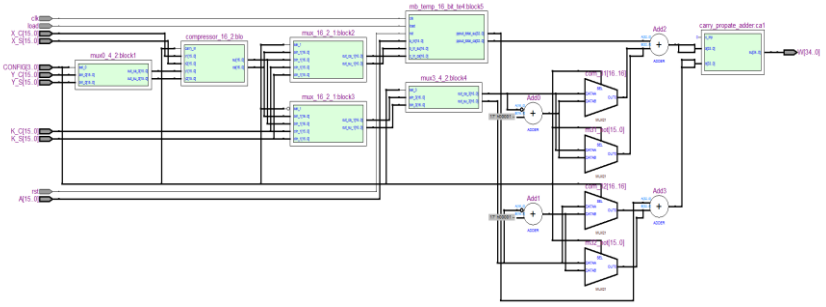

Fig 6. RTL view of Proposed FCU

V. CONCLUSION

The proposed a flexible accelerator architecture that exploits the incorporation of CS arithmetic optimizations to enable fast chaining of additive and multiplicative operations. We differentiate from previous works on flexible computational unit using addition and subtraction it takes in extra hardware. Proposed Architecture forms in FAMA an efficient design of DSP Acceleration and improving the area, energy consumption and reduce the hardware. It exploits the incorporated features of the proposed units and enables fast computations, high operation densities and advanced data reusability

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